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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Hans Jurgen Mattausch, Koji Kishi, Nobuhiko Omori

Application No./Patent No.: 6,845,429 Filed/Issue Date: January 18, 2005

Entitled: MULTI-PORT CACHE MEMORY

Intellectual Ventures Fund 35 LLC (Name of Assignee) , a Limited Liability Company (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. [x] the assignee of the entire right, title, and interest; or

2. [ ] an assignee of less than the entire right, title and interest.
(The extent (by percentage) of its ownership interest is _____ %)

in the patent application/patent identified above by virtue of either:

A. [ ] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

OR

B. [x] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: Inventors To: President of Hiroshima University
The document was recorded in the United States Patent and Trademark Office at
Reel 012048, Frame 0552, or for which a copy thereof is attached.

2. From: President of Hiroshima University To: Hiroshima University
The document was recorded in the United States Patent and Trademark Office at
Reel 020666, Frame 0818, or for which a copy thereof is attached.

3. From: Hiroshima University To: Hiroshima University
The document was recorded in the United States Patent and Trademark Office at
Reel 020666, Frame 0830, or for which a copy thereof is attached.

[x] Additional documents in the chain of title are listed on a supplemental sheet.

[x] As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature	10/17/08 Date
Chun M. Ng Printed or Typed Name	(206) 359-8000 Telephone Number
Attorney for Assignee Title	

STATEMENT UNDER 37 CFR 3.73(b) - Supplemental Sheet

Continuation of chain of title from the inventor(s) to the current assignee.

4. From: President of Hiroshima University To: Hiroshima University
The document was recorded in the United States Patent and Trademark Office at
Reel 020666 , Frame 0947 , or for which a copy thereof is attached.

5. From: Hiroshima University To: Intellectual Ventures Fund 35 LLC
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

6. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

7. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

8. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

9. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____ , Frame _____ , or for which a copy thereof is attached.

EXHIBIT B
ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Hiroshima University, a Japanese educational institution, with an office at 1-3-2 Kagamiyama, Higashi-Hiroshima City, JAPAN 739-8511, ("***Assignor***"), does hereby sell, assign, transfer, and convey unto Intellectual Ventures Fund 35 LLC, a Nevada limited liability company, with an office at 7251 W Lake Mead Blvd, Ste 300, Las Vegas, NV 89128 ("***Assignee***"), or its designees, all right, title, and interest that exist today and may exist in the future in and to any and all of the following (collectively, the "***Patent Rights***"):

(a) the provisional patent applications, patent applications and patents listed in the table below (the "***Patents***");

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, (ii) for which any of the Patents directly or indirectly forms a basis for priority, and/or (iii) that were co-owned applications that directly or indirectly incorporate by reference the Patents;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all foreign patents, patent applications, and counterparts relating to any item in any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(e) all items in any of the foregoing in categories (b) through (d), whether or not expressly listed as Patents below and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(f) all inventions, invention disclosures, and discoveries described in any item in any of the foregoing categories (a) through (e) and all other rights arising out of such inventions, invention disclosures, and discoveries;

(g) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (f), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(h) all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or any item in any of the foregoing categories (b) through (g), including, without limitation, all causes of action and other enforcement rights for

(i) damages,
(ii) injunctive relief, and
(iii) any other remedies of any kind

for past, current, and future infringement; and

(i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (b) through (h).

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
3177637 (09-022805)	JP	4/13/2007 (2/5/1997)	Pulse width modulation operation circuit Iwata Atsushi; Nagata Makoto

5,889,424 (09/018,836)	US	3/30/1999 (2/4/1998)	Pulse width modulation operation circuit Iwata Atsushi; Nagata Makoto
2879670 (09-078025)	JP	1/29/1999 (3/28/1997)	Apparatus for processing two-dimensional information Iwata Atsushi; Nagata Makoto
6,088,490 (09/047,378)	US	7/11/2000 (3/25/1998)	Apparatus for processing two-dimensional information Iwata Atsushi; Nagata Makoto
3177636 (09-022804)	JP	4/13/2001 (2/5/1997)	Pulse modulation operation circuit Iwata Atsushi; Nagata Makoto
6,157,672 (09/018,837)	US	12/5/2000 (2/4/1998)	Pulse modulation operation circuit Iwata, Atsushi; Nagata, Makoto
6,845,429 (09/919,859)	US	1/18/2005 (8/2/2001)	Multi-port cache memory Hans Jurgen Mattaucsh; Kishi Koji; Omori Nobuhiko
01118905.7	EP	8/3/2001	Multi-port cache memory Hans Jurgen Mattaucsh; Kishi Koji; Omori Nobuhiko
90119391	TW	8/8/2001	Multi-port cache memory Hans Jurgen Mattaucsh; Kishi Koji; Omori Nobuhiko
10-2001-0048243	KR	8/10/2001	Multi-port cache memory Hans Jurgen Mattaucsh; Kishi Koji; Omori Nobuhiko
6,516,392 (09/533,336)	US	2/4/2003 (3/23/2000)	Address and data transfer circuit Hans Jurgen Mattaucsh
60003482 (20006003482)	DE	(3/24/2000)	Address and data transfer circuit Hans Jurgen Mattaucsh
EP1039475 (FR00106456.7)	FR	6/25/2003 (3/24/2000)	Address and data transfer circuit Hans Jurgen Mattaucsh
EP1039475 (GB00106456.7)	GB	6/25/2003 (3/24/2000)	Address and data transfer circuit Hans Jurgen Mattaucsh
EP1039475 (IT00106456.7)	IT	6/25/2003 (3/24/2000)	Address and data transfer circuit Hans Jurgen Mattaucsh
10-2000-0015127	KR	3/24/2000	Address and data transfer circuit Hans Jurgen Mattaucsh
89105448	TW	3/24/2000	Address and data transfer circuit Hans Jurgen Mattaucsh
0350525	KR	8/16/2002	Shared memory

		(2/11/2000)	Hans Jurgen Mattaucsh
89101956	TW	2/3/2000	Shared memory Hans Jurgen Mattaucsh
EP1033722 (FR00102565.9)	FR	10/12/2003 (2/7/2000)	Shared memory Hans Jurgen Mattaucsh
EP1033722 (GB00102565.9)	GB	10/12/2003 (2/7/2000)	Shared memory Hans Jurgen Mattaucsh
EP1033722 (IT00102565.9)	IT	10/12/2003 (2/7/2000)	Shared memory Hans Jurgen Mattaucsh
DE60007010 (DE20006007010)	DE	10/12/2003 (2/7/2000)	Shared memory Hans Jurgen Mattaucsh
6,874,068 (09/500,254)	US	3/29/2005 (2/8/2000)	Shared memory Hans Jurgen Mattaucsh
7,035,875 (10/296,224)	US	4/25/2006 (6/1/2001)	Method of using multi-media information, system and program recording medium therefor Kodama Mei
3555756 (2000-169459)	JP	(6/6/2000)	Multimedia information utilizing method, recording medium recording multimedia information utilizing program and multimedia information system KODAMA AKRIA
01936836.4	EP	06/01/2001	Method of using multi-media information, system and program recording medium therefor Kodama Mei
7,098,682 (10/497,514)	US	8/29/2006 (12/3/2002)	Testing method and tester for semiconductor integrated circuit device comprising high-speed input/output element Sasaki Mamoru
02824261.0	CN	12/3/2002	Testing method and tester for semiconductor integrated circuit device comprising high-speed input/output element Sasaki Mamoru
10-0571312	KR	4/10/2006	Testing method and tester for semiconductor integrated circuit device comprising high-speed input/output element Sasaki Mamoru
3446124 (2001-370609)	JP	(12/14/2001)	Testing method and tester for semiconductor integrated circuit device comprising high-speed input/output element Sasaki Mamoru

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Hiroshima Japan on March 31, 2008.

ASSIGNOR:

Hiroshima University

By: Toshiyuki Shimizu
Name: Toshiyuki Shimizu
Title: Executive (Finance) Member of Board of Directors; Authority for Contracts
(Signature MUST be attested)

ATTESTATION

The undersigned witnessed the signature of Toshiyuki Shimizu to the above Assignment of Patent Rights on behalf of Hiroshima University and makes the following statements:

1. I am over the age of 18 and competent to testify as to the facts in this Attestation block if called upon to do so.

2. Toshiyuki Shimizu is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on ~~April~~ March 31, 2008 to execute the above Assignment of Patent Rights on behalf of Hiroshima University. E.U

3. Toshiyuki Shimizu subscribed to the above Assignment of Patent Rights on behalf of Hiroshima University.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.
EXECUTED on March 31, 2008 (date)

Print Name: Eiji Ueda